OPERATION AND SERVICE MANUAL

MODEL 900 VLF/LF RECEIVER

19359

June 1973

Tracor, Inc.

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Tracor, Inc.

TRACOR 6500 TRACOR LANE, AUSTIN, TEXAS 78721

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SECTION I

INTRODUCTION

The Model 900 VLF/LF Receiver is used to keep track of the offset of a precision local frequency standard with respect to the accurately stabilized carrier frequency of one of the VLF or LF transmitters operated by NBS or by the United States Navy. VLF carriers are typically synthesized from Cesium Beam Frequency Standards located at the transmitters; a long-term frequency accuracy at least as good as one part in $(10)^{11}$ will normally be exhibited by the VLF carrier.

SECTION II

UNPACKING AND INSPECTION

Carefully unpack the receiver and inspect it for possible damage during shipment. Special attention should be given to any areas where the outside shipping package was damaged. If the frequency standard is damaged in any way, immediately notify the carrier. Also notify TRACOR, Inc., 6500 Tracor Lane, Austin, Texas 78721, 512/926-2800 Attention: Product Service.

SECTION III

INSTALLATION AND OPERATION

Installation and Operation

Use of the receiver is quite simple. Mount the antenna in a clear outdoor area, such as a rooftop. Other conducting objects should be kept at least four feet away from the antenna, and there should be no conductors (such as power lines) at a high elevation angle as viewed from the antenna position.

Connect the antenna coupler to the receiver ANTENNA connector using the coaxial cable provided. Connect 1 MHz (100 kHz optional) from the frequency standard being monitored to the 1 MHz connector of the receiver.

Plug the power cord into a receptacle providing 105-125 volts, 60 Hz. (Operation at 220 V and/or 50 Hz available on special order.)

Initially select a strong nearby transmitter, even if it is desired later to use a different transmitter. Place the VLF/LF switch in VLF position, and set the FREQUENCY switches as shown in Table 1 for the selected transmitter. Within the United States NAA, NLK, or NSS will provide strong signals. Other transmitters not shown in the table may be on at a later date, and in particular there will be a wide selection of transmissions from the various OMEGA transmitters. For a general method of tuning transmitters not shown in the table see page 17.

Turn the front panel GAIN control fully counter-clockwise. The indicator lamp should be extinguished. Turn the GAIN control

TABLE 1

SWITCH SETTINGS FOR VARIOUS TRANSMITTERS

Transmitter	Location	XMTR Freq.	SYNTH Freq.	VLF/LF Switch	Frequency Switches
OMEGA	Trinidad				
GBR	England	16.0	15.5	VLF	U D D U U U U U
NAA	Maine	17.8	17.7	VLF	U D U U D D D U
NLK	Wash State	18.6	18.5	VLF	U D U U U D D U
NSS	Maryland	21.4	21.3	VLF	U U D U D U D U
NWC	Australia	22.3	22.2	VLF	U U D U U U U D
NBA	Canal Zone	24.0	23.9	VLF	U U U D U U U U
WWVL	Colorada	60.0	9.9	LF	D U U D D D U U
MSF	England	60.0	9.9	LF	D U U D D D U U
HBF	Switzerland	75.0	24.9	LF	U U U U U D D U

slowly clockwise. At some point the indicator lamp should come on or begin to blink on and off. When this point is reached, turn the control an additional 1/10 turn clockwise. This provides the optimum gain for the selected transmitter and insures proper reception even though the received signal level should change over a 20 dB range.

Any given transmitter may occasionally be shut down temporarily for maintenance. In the absence of reception from the originally selected transmitter, try a second transmitter.

When a transmitter is first received, the chart recorder needle should move steadily over a period of some 10 seconds to one minute and reach a position where it remains fairly stationary.

For a strong signal the indicator light should come on well below the maximum GAIN position. At maximum gain the lamp may flicker as a result of atmospheric noise reception. When reception is normal, and the GAIN setting proper, switching the third FREQUENCY switch from the right away from the correct position should usually cause the indicator lamp to go out. Keep a record of gain setting for each transmitter normally used. This will be a useful guide in recognizing later transmitter shutdowns.

Various chart indications of proper tracking will become familiar after a few days of operation. The diurnal shift pattern is one such indicator. The CEC reading should increase gradually as the sunset line moves westward along the path between transmitter and receiver. The CEC decreases at sunrise may not be smooth and gradual.

Chart Recorder Adjustments

The chart recorder should be checked occasionally for correct zero and full-scale indications. Depress the RCDR ZERO toggle on the front panel. The recorder should now give a reading of zero. If not, adjust the recorder mechanical zero.

Next depress the FULL SCALE toggle. The recorder should now read 100 CEC. If not, adjust the RCDR FS ADJ available through the front panel access hole.

Choice Of A Transmitter

Normally the transmitter providing the strongest signal will be selected for continuous frequency monitoring. In some

cases a transmitter at a particular short range may give erratic results at sunrise. Try each of several strong transmitters for a period of several days and select one with a stable diurnal shift pattern.

Interpretation of Chart Records

Frequency offset of the local frequency standard with respect to the VLF carrier is determined from the chart record produced by the receiver. In general the offset is determined as follows:

Let Δt be the phase change noted on the chart expressed in microseconds.

Let ΔT be the elapsed time interval over which the change occurs, expressed in seconds. The fractional frequency offset is then

$$\frac{\Delta t}{\Delta T} \quad X \quad (10)^{-6}$$

In other words, a phase rate of one microsecond per second corresponds to a fractional frequency deviation of 1 part in $(10)^6$.

Δt is determined from the chart record. Full scale deflection corresponds to 1 cycle of phase at the VLF carrier. It will prove most convenient to read phase change in hundredths of a cycle, or centicycles, and then convert to microseconds. At 17.8 kHz, for example, the frequency transmitted from Cutler, Maine, full scale is 56.2 microseconds. To convert from CEC to μs multiply by 0.562. Suppose, for example, that over a 24-hour

period from noon to noon, the phase reading increases by 7 CEC. This corresponds to 7 x 0.562 = 3.9 μs. Twenty-four hours is 86,400 seconds. So the fractional frequency offset is

$$\frac{3.9}{8.64(10)^4}(10)^{-6} = 4.5 \times 10^{-11}$$

An increasing phase reading indicates that the local frequency is high. A decreasing phase reading indicates that the local frequency standard is low in frequency.

C_A_U_T_I_O_N

THE FOREGOING DETERMINATION OF WHETHER THE LOCAL STANDARD IS HIGH OR LOW IN FREQUENCY ASSUMES THAT THE SYNTHESIZED LOCAL OSCILLATOR SIGNAL IS 100 HZ BELOW THE CARRIER AS RECOMMENDED IN THE OPERATING INSTRUCTIONS AND SET-UP TABLES IN THIS MANUAL. IF RECEPTION IS EFFECTED BY PLACING THE LOCAL OSCILLATOR 100 HZ ABOVE THE CARRIER, THE SENSE OF THE READOUT WILL BE REVERSED.

Figure 1 gives in graphic form the conversion from centicycles to microseconds, while figure 2 permits graphic determination of fractional frequency offset.

Several facts must be understood in order to interpret properly the receiver records. First of all, propagation time from the transmitter to the receiver is not precisely constant. In particular, there is a marked difference between daytime and nighttime delay. This change is known as the "diurnal shift" and results from the change in the height of the ionosphere. Nighttime propagation is slower than daytime propagation by some tens of microseconds. The delay is most stable when the entire path is in daylight. Repeatability from day to day is usually accurate to approximately one microsecond. At night

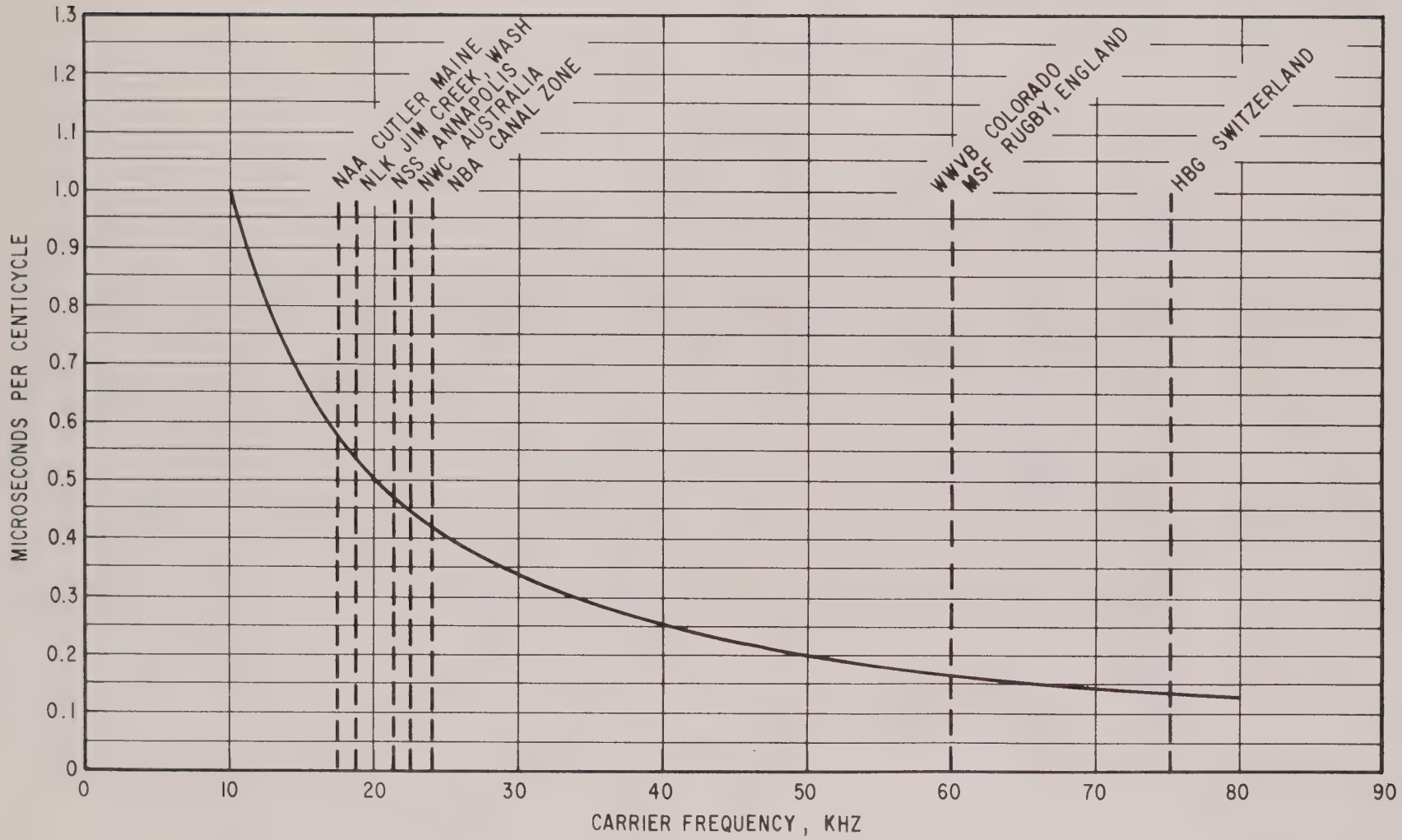


FIGURE I CONVERSION FROM CENTICYCLES TO MICROSECONDS

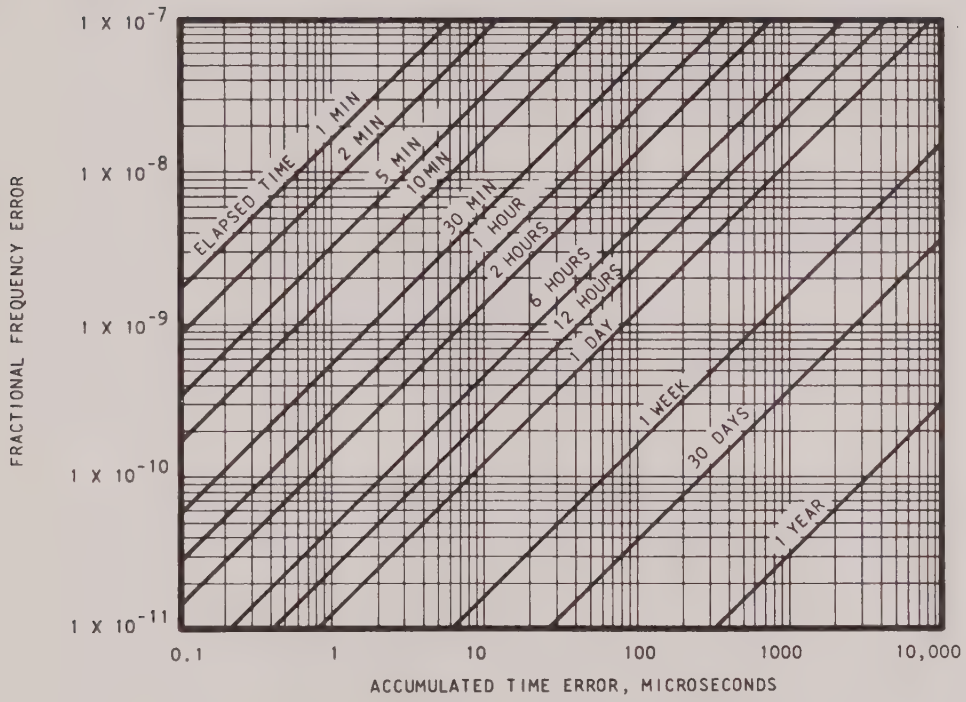


Figure 2 Fractional Frequency Error Chart

random fluctuation of five to ten microseconds or more often occur. Thus the best results are obtained by taking readings at the same time each day; the time selected should be one during which the transmission path is entirely in daylight. The entire chart should be examined in the neighborhood of the selected time to insure that the appearance is normal. This is desirable because occasionally a solar flare can affect propagation delay for an hour or two, and a reading taken during such a time interval would lead to inferior results. With care, an accuracy approaching one microsecond can be achieved over a period of one day. This results in a frequency measurement accuracy approaching 1 part in $(10)^{11}$.

Fortunately frequency standards which are sufficiently stable to make readings to a part in $(10)^{11}$ meaningful are also stable enough so that a day's elapsed time does not result in a change in frequency which is much greater than a few parts in $(10)^{11}$. Or, to put it another way, if a standard shifts so rapidly that a measurement must be made in a period much shorter than one day, then an accuracy of parts in $(10)^{11}$ is seldom required. Utilizing a period of all-daylight reception, a frequency determination at least as good as one part in $(10)^{9}$ can usually be achieved in an hour or two.

Figure 3, 4, and 5 are three representative chart recordings from the Model 900 Receiver.

Figure 3 shows reception of WWVB, 60 kHz. Note the gradual increase of phase after 4 PM at the right hand edge of the upper strip chart record and the left hand edge of the center record. This is the evening diurnal shift.

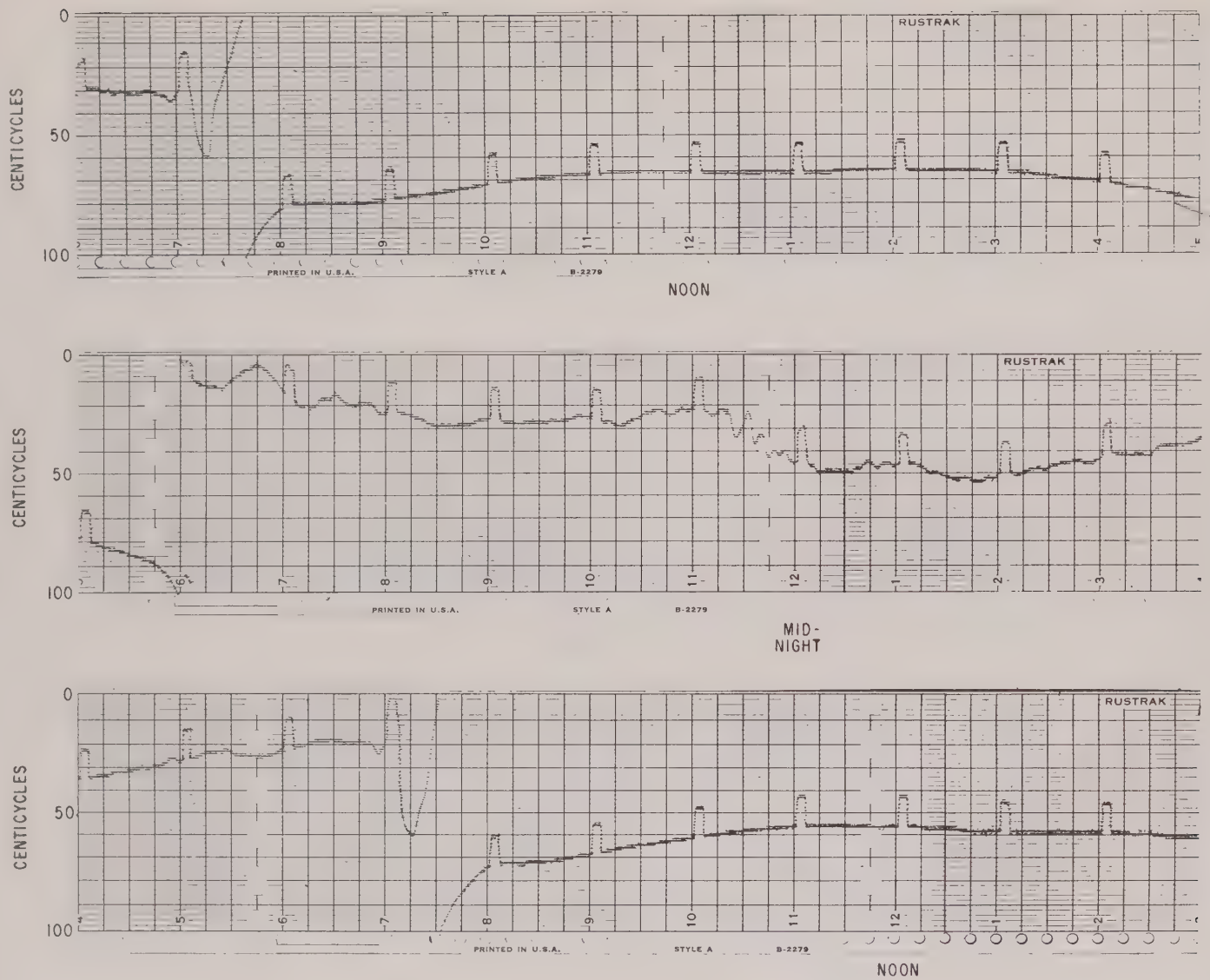


FIGURE 3 WWVB (60KHZ) AS RECEIVED AT AUSTIN, TEXAS
OSCILLATOR OFFSET APPROXIMATELY -2.3×10^{-11}

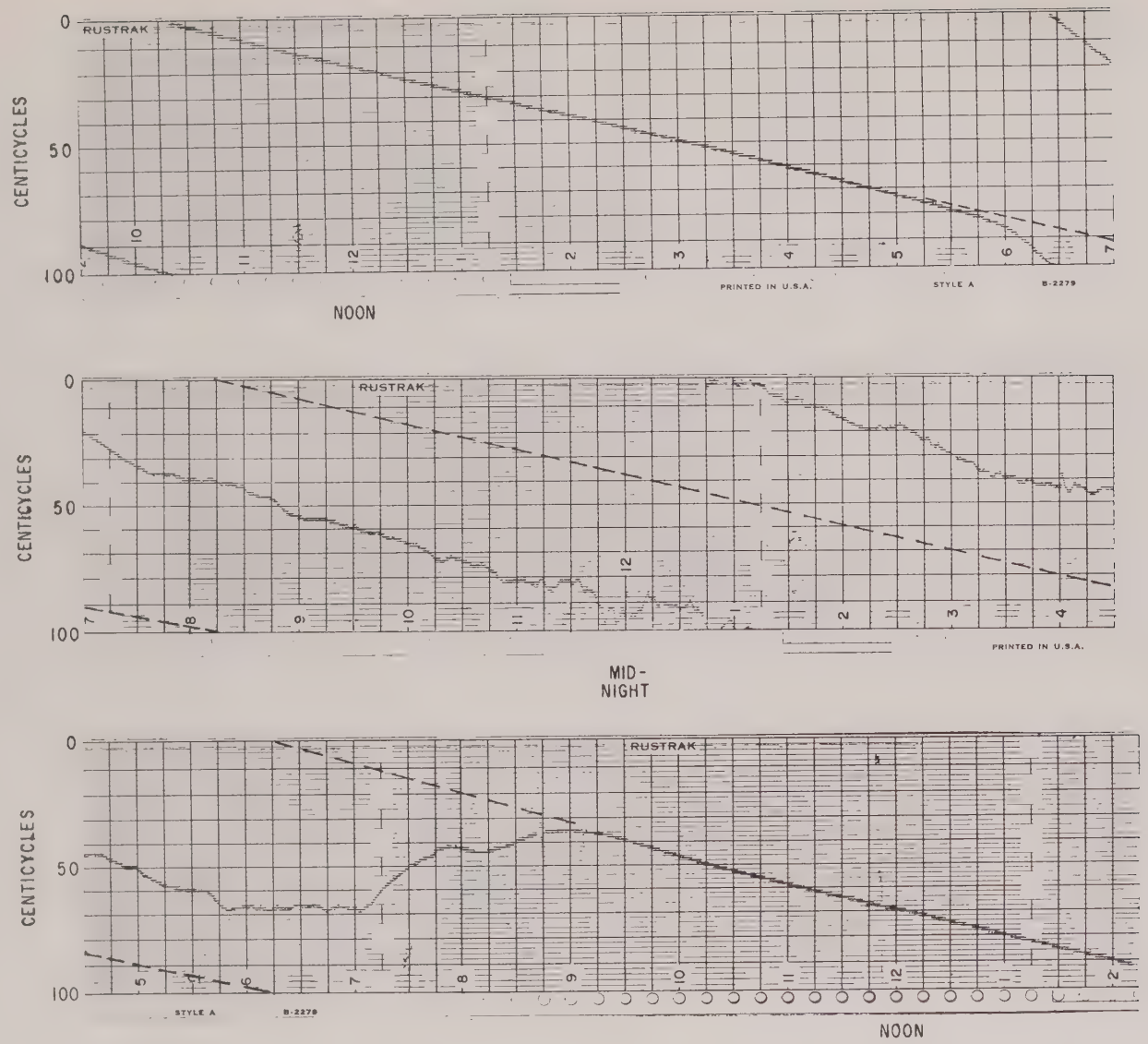


FIGURE 4 NLK (18.6 KHZ) AS RECEIVED AT AUSTIN, TEXAS
OSCILLATOR OFFSET APPROXIMATELY + 1.6 x 10^{-9}

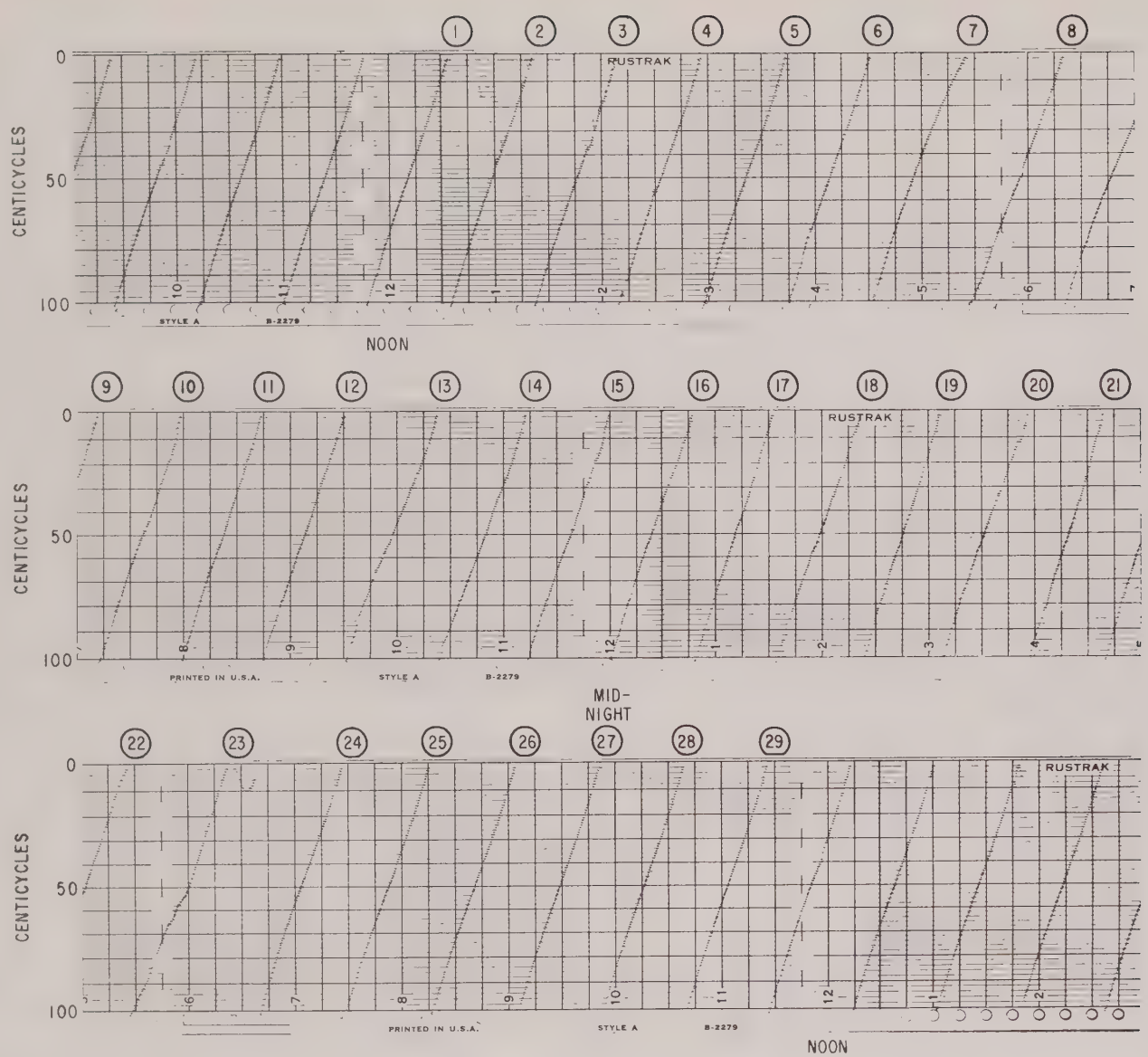


FIGURE 5 NAA (17.8KHZ) AS RECEIVED AT AUSTIN, TEXAS
OSCILLATOR OFFSET APPROXIMATELY -1.9×10^{-8}

Note also the apparent sudden jump from 100 CEC to 0 CEC at 9 PM near the left of the center strip. The total range of the phase detector is 100 CEC, or one full cycle of phase, When one extreme is reached the record reverts to the other extreme. If the phase just before 9 PM is 99 CEC, the phase just after 9 PM is obviously not 1 CEC, but 101 centicycles. It is necessary to count cycle accumulation in this fashion when reading a chart record. This will become clearer in the two later examples.

The sunrise effect between 7 and 8 AM on the lower strip is not so smooth and gradual as the evening shift. Looking at this area alone, it might not be easy to determine whether a cycle could perhaps have been gained or lost. Looking at the daytime record, however, it is clear that there is approximately zero average slope so that the record returns to the same cycle the second day as the first.

Note also that the daylight record is rather smooth, while the nighttime record "wanders" back and forth a number of centicycles in the course of an hour or two.

Note also the phase shift lasting approximately five minutes of each hour. This shift is introduced at the WWVB transmitter. Its presence in the recording is a definite indication of proper phase tracking.

At noon the first day the reading is 67 CEC. At noon the second day the reading is 56 CEC. The 24 hour change is then 56 - 67 = -11 CEC.

Referring to figure 1, at 60 kHz the number of microseconds per centicycle is 0.167. The change expressed in microseconds then is

$$0.167\ (-11) = -1.837\ \mu s.$$

Referring to figure 2, 1.837 μs in 24 hours is an offset of 2.3 parts in $(10)^{11}$. Since the change is negative the local frequency standard was low by 2.3 parts in $(10)^{11}$

Figure 2 shows reception of NLK, Jim Creek, Washington, at 18.6 kHz. Here there is an obvious gradual phase increase with time. The evening shift beginning about 6 PM is easily recognized. The smooth daytime and more variable nighttime characteristics are obvious. The sunrise shift in this case is fairly smooth.

Clearly there is a cycle change near 6:30 PM the first day, and near 1 AM. The reading at noon the first day is 17 CEC. Clearly by noon the second day two additional cycles have been accumulated and the reading is taken not simply as 69, but as 269. A dashed line has been added showing a continuation of the steady daytime slope. This verifies that exactly two cycle changeovers have occurred.

The change is 269 - 17 = 252 CEC. From figure 1, at 18.6 kHz one CEC is 0.54 μs, so the 24 hour change is

$$(253)(0.54) = +137\ \mu s$$

From figure 2 this represents a frequency offset of 1.6×10^{-9} Since the change is positive the oscillator frequency is high.

An approximation could have been obtained over a shorter period of time. At 2 PM the first day the reading is 38 CEC. The change since noon is then

$$38 - 17 = 21 \text{ CEC, or}$$
$$(21)(0.54) = 11.3 \ \mu s$$

By calculation 11.3 μs in 2 hours is

$$\frac{11.3}{(2)(3600)} \times 10^{-6} = 1.7 \times 10^{-9}$$

This last result could, of course, be obtained from Figure 2 instead of making the calculation.

Figure 5 illustrates a more radical oscillator offset. From noon the first day to noon the second there are 29 cycle crossovers. These have been numbered on the chart reproduction. Since the reading is decreasing it is easiest to take the final reading as 30 CEC. The initial reading is then 2973, and the change is -2943.

From Figure 1, at 17.7 kHz, 1 CEC is 0.56 μs. The change is (-2943)(0.56) = - 1655 μs. This corresponds to a frequency offset of 1.9×10^{-8}.

With so great an offset, there is normally little to be gained by seeking the accuracy inherent in a 24 hour reading. For example, there is a complete cycle between 11 on the first day and about 11:47. 100 CEC is 56 μs. 56 μs in 47 minutes is, from figure 1, about 1.8×10^{-8}.

Calculation of Frequency Switch Settings

The most frequently used frequency settings have been given in Table 1. It is relatively easy to calculate any desired setting. The switches select the frequency in binary form as follows:

	Switch	Binary Value (multiple of 100 Hz)
(LEFT)	S208	128
	S207	64
	S206	32
	S205	16
	S204	8
	S203	4
	S202	2
(RIGHT)	S201	1

When the switch is UP, the corresponding number is added in. With the switch DOWN, the number is omitted.

Suppose, for example, that it is desired to select 18.5 kHz in order to receive the VLF carrier at 18.6 kHz. The desired multiple of 100 Hz is 185. S208 is placed up contributing 128 toward the required 185. The difference 185 - 128 = 57 must be supplied by the remaining switches. Clearly 64 would be too much, so S207 is placed down, omitting 64. S206 is placed up, providing 32 of the required 57. The remaining switches must supply 57 - 32 = 25. S205 is placed up, providing 16, and leaving a requirement for 9. S204 is placed up supplying 8 of the 9. S203 and S202 are then placed down, while S201 is placed up, providing the last 1. To summarize in tabular form:

S208	128	X1 (UP)	=	128
S207	64	X0 (DOWN)	=	0
S206	32	X1 (UP)	=	32
S205	16	X1 (UP)	=	16
S204	8	X1 (UP)	=	8
S203	4	X0 (DOWN)	=	0
S202	2	X0 (DOWN)	=	0
S201	1	X1 (UP)	=	1
		TOTAL		185

SECTION IV

THEORY OF OPERATION

A block diagram of the Model 900 LF/VLF Receiver is given in figure 6.

The signal is received by a vertical whip antenna mounted on the antenna coupler unit. A pre-amplifier in the coupler provides approximately unity voltage gain while converting the impedance to a level which can drive the 50-ohm cable feeding the main receiver unit.

With the LF/VLF switch in VLF position the signal goes directly to the R-F amplifier. (For LF reception the signal is converted down by mixing with a 50 kHz local oscillator signal.) Another local oscillator signal is synthesized at a frequency 100 Hz below the desired VLF signal frequency. Mixer action converts the r-f signal to 100 Hz for amplification by an I-F amplifier tuned to 100 Hz.

The 1 MHz signal from the frequency standard being tested is used to produce signals at various frequencies including the local oscillator signals at 50 kHz and at f_o - 100 Hz. Two signals are produced at 100 Hz, one by simple division, the other by a divider circuit which includes provision for adding inhibiting pulses, thus advancing or retarding the phase of the resulting 100 Hz. The shifted 100 Hz signal is used as a reference signal in a synchronous detector. If the phase difference between the 100 Hz reference and the 100 Hz I-F signal is exactly 90°, no error signal is produced and the phase of the

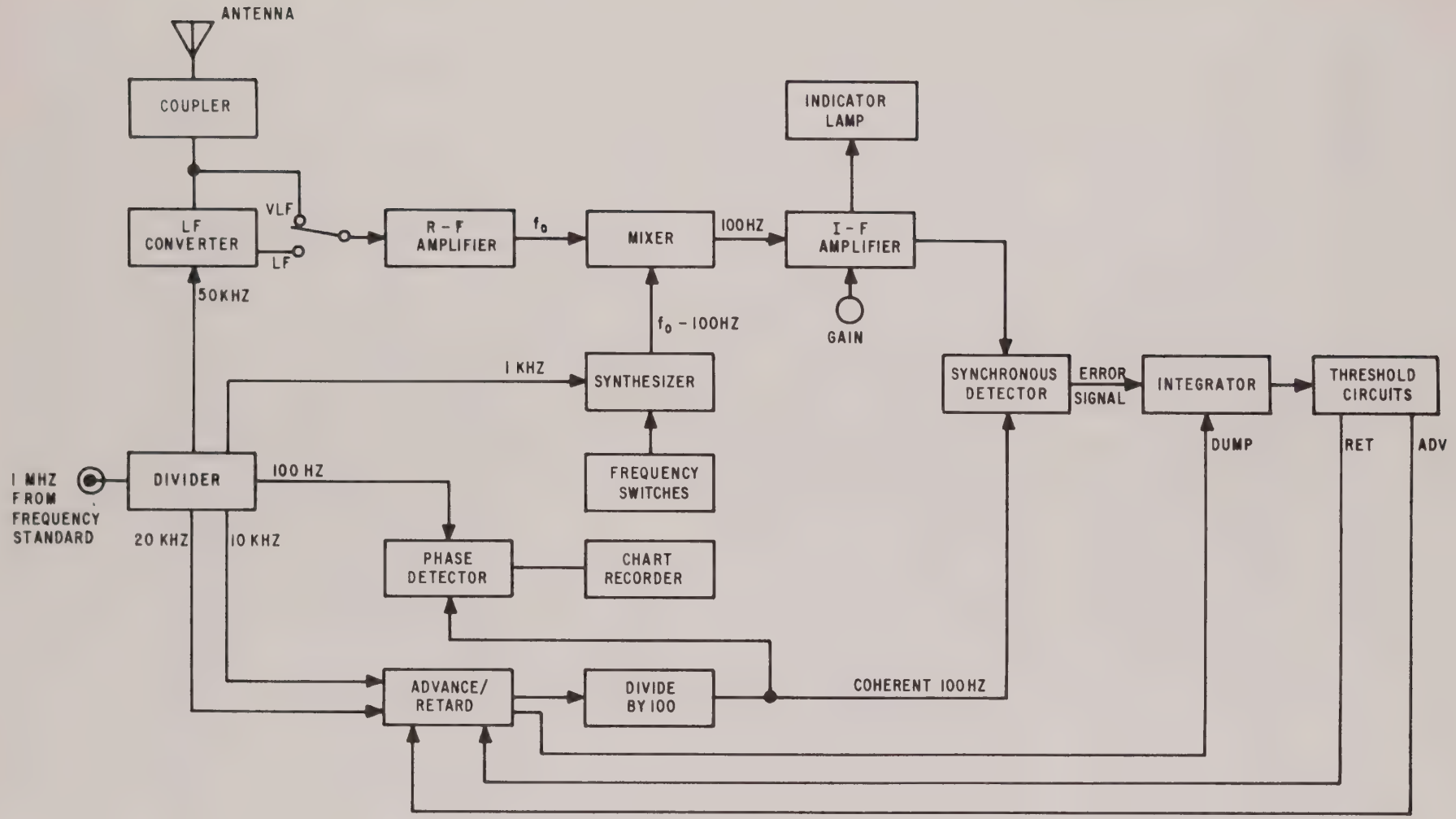


Figure 6. Block Diagram, VLF Receiver Model 900

reference signal is maintained constant. If the phase difference is temporarily less than 90°, retard pulses are repeatedly generated until the phase difference is 90°. If the phase difference is temporarily greater than 90°, repeated advance pulses are generated. Thus closed loop action phase locks the coherent 100 Hz signal 90° away from the I-F signal phase.

Any phase change in the received signal thus results in a corresponding phase change in the coherent 100 Hz signal. Phase comparison of the coherent 100 Hz with respect to the fixed-phase 100 Hz signal produced by direct division provides a chart recorded signal representation of the phase of the incoming VLF carrier (with reference to the local frequency standard). The change in phase measured over a period of one day then serves to indicate the amount of frequency offset existing in the local standard with respect to the atomic frequency standard being used to stabilize the VLF transmission.

Detailed Circuit Theory

Antenna Coupler

Figure is a schematic of the antenna coupler. FET Q1 is a high-input impedance low-noise amplifier as required by the high-impedance whip antenna. A surge voltage limiter and two back-to-back zener diodes are included in the input circuitry to protect the other circuit elements from high voltage surges caused by nearby lightning strikes. RC filtering attenuates signals above 100 kHz.

Amplifiers Q2 and Q3 provide additional gain, while emitter follower Q4 provides a low output impedance to drive the

cable feeding the main receiver. DC voltage is supplied via the center conductor of the coxial cable.

Figure is a schematic diagram of the receiver proper. For convenience the circuits are subdivided into sections as follows:

Section Title	Typical Reference Designator
Divider	R101
Synthesizer	R201
Synchronous Detector	R301
R-F/I-F	R401
Power Supply	R501
LF-to-VLF Converter	R601

Each circuit group occupies a separate section of the printed circuit card.

R-F/I-F Circuits

The signal from the antenna coupler enters at TP405. Power for the coupler is supplied through R446. L401 and C420 provide additional rejection of signals above 100 kHz.

With S501 in VLF position the incoming signal goes directly to amplifier U401, pin 3. Two amplifier sections with a total voltage gain of approximately 200 precede the mixer Q404. The synthesizer signal at the gate of Q404 is chosen 100 Hz below the VLF carrier producing an output to U402, pin 11 at a frequency of 100 Hz. After amplification by three sections of U402 the signal reaches an active bandpass filter (U403D, C410, C411, R424, etc.). This stage is tuned to 100 Hz with a Q of approximately 10.

The next section of U403(C) feeds a limiter (CR1, CR2, etc.) which insures constant level I-F signal at the synchronous detector. The limited signal is amplified in the final section of U403(B) and applied to the synchronous detector section via emitter follower Q403.

Q401 acts as a detector and amplifier for the signal. Amplifier Q402 drives indicator lamp DS1. In the absence of I-F signal DS1 is dark. With adequate I-F signal present DS1 is lit. DS1 thus serves as a guide in setting gain control R416 to provide adequate but not excessive I-F signal level.

For LF reception the signal is amplified by Q601 and Q602. High pass filter L602, 609, etc. rejects possible very strong VLF signals which might pass directly through and interfere with the desired LF signal reception. The LF signal is mixed with 50 kHz at mixer Q603. An LF signal at 60 kHz, for example, would then produce an output at 10 kHz at the junction of R614 and C615. The filter consisting of C615, R617, etc. notches out the 50 kHz local oscillator signal. The filter output goes to U401, via S501 in the LF position.

Divider Circuit Group

The 1 MHz signal from the frequency standard enters at E101, and is buffered and shaped by Q101 and U105A. The shaped 1 MHz serves as a clock signal for a divider chain consisting of decade dividers U101, 102, 103, and 104 which produce 100 kHz, 10 kHz, 1 kHz and 100 Hz respectively.

The 100 kHz signal from U101 is frequency divided by 2 to 50 kHz by J-K flip flop U107B. The 50 kHz output is used as the local oscillator signal for mixing LF signals (such as 60 kHz) down to the VLF band.

U102 receives 100 kHz at pin 1 and frequency divides by 5, producing 20 kHz at pin 11. This 20 kHz signal is fed back into the divide by 2 section at pin 14, producing 10 kHz at pin 12.

The 20 kHz signal at U102, pin 11 and the 10 kHz signal at U102, pin 12 are utilized in the ADVANCE/RETARD circuit. The two signals are fed together to NAND gate U105B. The output of U105B is ground only when both the 20 kHz signal and the 10 kHz signal are positive. The result is a negative pulse of 25 µs duration occurring each 100 µs at U105, pin 6.

Similarly the 20 kHz signal is combined with an inverted version of the 10 kHz signal at U105D to produce a second 25 µs pulse displaced 25 µs in time from the first, at U105, pin 11.

As will be shown presently, the "retard gate" line at U106, pin 2 is normally negative. Thus the output at U106, pin 1 goes positive for 25 µs of each 100 µs. The "advance gate" line at U106, pin 5 is normally positive, holding U106, pin 4 continuously at ground. Under these conditions the signal at U106, pin 13 is positive for 75 µs of each 100 and negative for 25 µs of each 100. the repetition period is, of course, 10 kHz. The 10 kHz signal is frequency divided to 100 Hz by U108 and U109.

Each output from U109 triggers one-shot U111. The period of the one-shot is just over 100 µs, or one cycle at 10 kHz. A

positive pulse is produced at pin 6 which feeds U113B. A negative pulse at pin 1 feeds U112A. If a positive signal exists on the advance enable input at U113, the occurrence of the positive pulse at pin 5 results in a negative pulse at U113, pin 6. This is applied as the advance gate at U106, pin 5. This permits the negative pulse at U106, pin 6 to create a positive pulse at U106, pin 4 and a negative pulse at U106, pin 13. The pulse at U106, pin 13 is in addition to the train of pulses normally passing at a 10 kHz rate through U106A and U106D. Thus an extra clock pulse is applied to U108, and the 100 Hz output signal at U109, pin 12 is advanced by 1/100 of a cycle, or one centicycle, of phase.

If a negative retard enable signal exists at U112, pin 3, the negative pulse from the one-shot at U112, pin 2 produces a positive pulse at U112, pin 1. This is fed as the retard gate to U106, pin 2. This positive signal inhibits passage of one pulse of the 10 kHz pulse train normally transmitted via U106A. This results in one lost clock pulse at U108, pin 1, and a phase retardation of 1 centicycle in the 100 Hz output from U109.

When either the positive or the negative one-shot pulse is enabled, a negative pulse results at U112, pin 13. This triggers one-shot U114 which produces a "dump pulse". Use of this dump pulse and the generation of the retard enable and advance enable signals will become clear in the later discussion of the synchronous detector circuits group.

U107A serves as a linear phase detector. The 100 Hz output of U109 which is phase locked to the received signals is phase compared with the 100 Hz output of U104 derived by direct division from the frequency standard. The output of U109 clocks the flip flop U107A to the $\overline{Q}$ zero state; a short one-shot pulse derived

from the 100 Hz output of U104 clears the flip flop to the $\overline{Q}$ positive state. If the clear pulse follows very quickly after the clock pulse $\overline{Q}$ is zero only a small fraction of one cycle at 100 Hz, and is positive the rest of the time. If there is a delay of nearly a full cycle between clock and clear, $\overline{Q}$ is zero nearly all the time. The DC level at $\overline{Q}$ is thus a linear measure of the relative phase between the 100 Hz signals from U109 and from U104.

This signal is applied via R103 and R104 to the chart recorder. S101 is a hold-to-open spring loaded toggle. When the toggle is actuated U107A is clocked to $\overline{Q}$ zero and is not again cleared to a $\overline{Q}$ positive as long as S101 is operated. S101 thus serves to ZERO the chart record. When spring loaded toggle S102 is held open U107A is cleared to $\overline{Q}$ positive and is not again clocked to $\overline{Q}$ zero. S102 thus serves as a FULL SCALE actuator for the recorder. While S102 is held open, the recorder deflection is adjusted for 100 CEC using variable resistor R104.

Power for the integrated circuits is obtained from 6-volt regulator U115 which in turn is powered via R107 and R108 from the 12 volt regulator in the main power supply circuit section.

Synthesizer Circuit Group

The synthesizer circuit which produces a signal 100 Hz below the received carrier consists basically of voltage controlled oscillator U202, phase comparator U201, and preset dividers U205 and U206. The dividers are set to divide the oscillator frequency by a number N. The oscillator frequency is controlled by the phase detector output so that the divider output f_{osc}/N is phase locked to the 1 kHz input. Then

$$f_{osc}/N = 1 \text{ kHz}$$

$$\text{or, } f_{osc} = N \times 1 \text{ kHz}$$

The oscillator signal is frequency divided by 10 in decade divider U204. The output frequency $f_{osc}/10$ is thus

$$f_{osc}/10 = N \times 100 \text{ Hz}.$$

Clearly then the synthesizer will produce any integral multiple N x 100 Hz which can be selected in U205 and U206. The maximum N is one less than 16 x 16, or 255, permitting direct reception of signals up to 25.6 kHz.

The dividers are loaded under control of the front panel FREQUENCY toggles. The dividers count down to zero and are then reloaded to the preselected number N by the output pulse at U205 pin 13 fed back to load inputs pin 11 of each counter.

The switches select the number N in binary form. Thus N = 128 corresponding to a synthesized frequency of 12.8 kHz would result from a switch setting of

S208	UP (1)
S207	DOWN (0)
S206	DOWN (0)
S205	DOWN (0)
S204	DOWN (0)
S203	DOWN (0)
S202	DOWN (0)
S201	DOWN (0)

This would be the desired setting for reception of a carrier at 12.9 kHz. See page 4 for a more detailed description of switch settings.

Synchronous Detector Circuit Group

The synchronous detector circuit group receives the I-F signal from the receiver circuit group and the shifted 100 Hz signal from the divider section. The I-F signal is shorted out via Q302 during one half-cycle of the 100 Hz reference. During the other half cycle the I-F signal is passed through to integrator circuit U302. If the reference signal is 90° out of phase with the I-F, equal positive and negative portions of the I-F signal are passed through, so net DC input to the integrator is zero (with respect to the 5-volt reference level).

If the reference signal at R304 is in phase with the I-F signal at C304, the I-F signal is shorted out during its negative half-cycle and passed during its positive half cycle. Thus a net positive DC (with respect to the 5-volt reference level) is supplied to the integrator. Similarly, if the reference is 180° out of phase with the I-F, a net negative signal reaches the integrator input.

If a positive input reaches the integrator, the integrator output runs gradually in a negative direction from the 5-volt reference level. When a voltage of approximately 3 volts is reached, voltage comparator U303A goes suddenly positive at output pin 4. This turns on Q306 producing a ground level retard enable signal in the divider section. As previously shown this causes the reference phase to be retarded by 1 CEC, and produces a negative "dump pulse". This dump pulse turns off Q304, which turns on FET Q303. This gives a direct low impedance feedback path across integrator capacitor C306, and quickly returns the output of U302, pin 6 to the 5-volt reference level.

If the 1 CEC phase shift is inadequate to bring the reference signal to quadrature with the I-F so that a positive polarity exists as before at the integrator input, the entire cycle just described is repeated. When successive phase retardations finally bring the reference to the other side of quadrature, a negative input to the integrator results, and the integrator output goes gradually positive. At about 7 volts it causes voltage comparator U303B output to go negative, cutting off Q305, and producing a positive advance enable signal. This results in a 1 CEC advance of the reference phase and a "dump pulse" to restore the integrator to 5 volts. In the steady state the reference signal goes from side to side of the quadrature position by a fraction of a centicycle, producing alternate advance and retard pulses.

Regulator U301 produces the 5-volt reference level used in the phase detector circuit section and also in the receiver section.

The power supply circuit which produces the regulated 12-volt supply for the various circuits is extremely simple. (See figure .) AC power is applied to T501. The secondary voltage goes to a bridge rectifier consisting of CR501 through CR504. The ripple is smoothed by C503, producing a DC input to R501 of approximately 32 volts (depending upon the exact line voltage). The current drain of the entire receiver is some ½ ampere. There is therefore a drop of some 15 volts across 30 ohms consisting of resistors R501, R502 and R503 in series permitting some 17 volts at the input of U501.

The LM309 holds the voltage between pins 2 and 3 at 5 volts. This results in 12 volts to ground at output pin 2.

SECTION V
REPLACEABLE PARTS

Ordering Information

Address orders or inquiries to either an authorized TRACOR, Inc., Sales Representative or to:

TRACOR, Inc.
Industrial Instruments
Customer Service
6500 Tracor Lane
Austin, Texas 78721

For prompt service, orders should include:

a. Name, model, and serial number of the instrument.
b. TRACOR stock number
c. Full description of the part.

Part numbers in Table 2 may change occasionally as items are reevaluated or as improved components become available. The part shipped will be the part used in production at the time the order is received, and will be equivalent to the part it replaces in both dimensions and performance.

TABLE 2

MODEL 900 VLF/LF RECEIVER
REPLACEABLE PARTS

Reference Designator	TRACOR Part No.	Description
	Power Supply (part of Cover Assy 19352-0001)	
C501	3403-9503	Cap Fxd Cer .05 UF
C502	3322-9102	Cap Fxd Cer .1 MFD
C503	23969-0005	Capacitor 3900 MFD
CR501	800-4002	Diode 1N4002
CR502	800-4002	Diode 1N4002
CR503	800-4002	Diode 1N4002
CR504	800-4002	Diode 1N4002
CR505	800-4002	Diode 1N4002
F501	3487-9752	Fuse .75 Amp 250 V
J1	3391-0002	Connector BNC Female
J2	3391-0002	Connector BNC Female
P501	3648-0008	Connector, Soc Elec
R501	76456-0002	Res 10 Ohm
R502	76456-0002	Res 10 Ohm
R503	76456-0002	Res 10 Ohm
R504	212-4640	Res Fxd Film 464 Ohm
R505	212-3320	Res Fxd Film 332 Ohm
R506		Resistor Selected

Reference Designator	TRACOR Part No.	Description
Power Supply, continued		
S501	23969-0881	Switch Toggle
T501	76367-0001	Transformer
TP501	3613-0037	Terminal Strip 5 Pin
TP502	3613-0037	Terminal Strip 5 Pin
TP503	3613-0040	Terminal Strip
TP504	3613-0040	Terminal Strip
U501	24142-0001	IC LM309K
W501	3467-0028	Cable, 3-Conductor
XF501	3488-0001	Fuseholder ¼ x 1¼
Antenna Coupler Assy 19348-0001		
J1	3391-0002	Connector BNC Female
J	19348-0001	PCB Assy Antenna Coupler
PCB Assy, Antenna Coupler 19348-0001		
C1	3321-9102	Cap Fxd Cer .1 MFD
C2	3321-9102	Cap Fxd Cer .1 MFD
C3	8914-0100	Cap Fxd Ta 10 MFD
C4	8914-0100	Cap Fxd Ta 10 MFD
C5	8914-0470	Cap Fxd Ta 47 MFD
C6	21485-9101	Cap Fxd Ta 1 MFD

Reference Designator	TRACOR Part No.	Description
PCB Assy, Antenna Coupler, continued		
C7	27512-0101	Cap Fxd Mica 100 PFD
C8	27512-0101	Cap Fxd Mica 100 PFD
C9	27512-0102	Cap Fxd Mica 1000 PFD
C10	27512-0102	Cap Fxd Mica 1000 PFD
C11	27512-0820	Cap Fxd Mica 82 PFD
C12	27512-0820	Cap Fxd Mica 82 PFD
E1	610-0093	Terminal, Solder
E2	610-0093	Terminal, Solder
E3	610-0093	Terminal, Solder
E4	610-0093	Terminal, Solder
E5	610-0093	Terminal, Solder
E6	18678-0001	Surge Voltage Protector
Q1	901-4221	Transistor, 2N4221A
Q2	900-2905	Transistor, 2N2905
Q3	900-2270	Transistor, 2N2270
Q4	900-2270	Transistor, 2N2270
R1	201-0101	Res Fxd Comp 100 Ohm
R2	204-0102	Res Fxd Comp 1.00K
R3	204-0103	Res Fxd Comp 10.0K
R4	204-0105	Res Fxd Comp 1.00 MEG
R5	204-0151	Res Fxd Comp 150 Ohm
R6	204-0153	Res Fxd Comp 15.0K
R7	204-0182	Res Fxd Comp 1.80K
R8	204-0102	Res Fxd Comp 1K
R9	204-0222	Res Fxd Comp 2.20K
R10	204-0271	Res Fxd Comp 270 Ohm

Reference Designator	TRACOR Part No.	Description
PCB Assy, Antenna Coupler, continued		
R11	204-0271	Res Fxd Comp 270 Ohm
R12	204-0273	Res Fxd Comp 27.0K
R13	204-0275	Res Fxd Comp 2.70 MEG
R14	204-0471	Res Fxd Comp 470 Ohm
R15	204-0472	Res Fxd Comp 4.70K
R16	204-0472	Res Fxd Comp 4.70K
R17	204-0472	Res Fxd Comp 4.70K
R18	204-0473	Res Fxd Comp 47.0K
R19	204-0332	Res Fxd Comp 3.3K
VR1	800-4747	Diode 1N4747
VR2	800-4747	Diode 1N4747

PCB Assy, Receiver 19308-0001

C101	3403-9103	Cap Fxd Cer .1 MFD
C102		Not Used
C103	27513-0102	Cap Fxd Mica 1000 PFD
C104	3324-9153	Cap Fxd Mylar .015 MFD
C105	21485-9101	Cap Fxd Ta 1 MFD
C106	3954-0016	Cap Fxd Elec 100 MFD
C107	3321-9102	Cap Fxd Cer .1 MFD
C109	3954-0016	Cap Fxd Elec 100 MFD
C110		Not Used
C111	3954-0016	Cap Fxd Elec 100 MFD
C112	3321-9102	Cap Fxd Cer .1 MFD
C113	3321-9102	Cap Fxd Cer .1 MFD
C114	3321-9102	Cap Fxd Cer .1 MFD
C115	3321-9102	Cap Fxd Cer .1 MFD

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
C201	3321-9102	Cap Fxd Cer .1 MFD
C202	23195-0043	Cap Fxd Ta 100.0 MFD
C203	3321-9102	Cap Fxd Cer .1 MFD
C204	23969-0009	Capacitor 1 MFD
C205		Not Used
C206	23195-0043	Cap Txd Ta 100.0 MFD
C207	3321-9102	Cap Fxd Cer .1 MFD
C208	3321-9102	Cap Fxd Cer .1 MFD
C209	27512-0182	Cap Fxd Mica 1800 PFD
C210	3321-9102	Cap Fxd Cer .1 MFD
C211	23195-0043	Cap Fxd Ta 100.0 MFD
C212	3321-9102	Cap Fxd Cer .1 MFD
C213	3321-9102	Cap Fxd Cer .1 MFD
C214	3321-9102	Cap Fxd Cer .1 MFD
C215	3321-9102	Cap Fxd Cer .1 MFD
C301	3322-9102	Cap Fxd Cer .1 MFD
C302	3954-0016	Cap Fxd Elec 100 MFD
C303	3321-9102	Cap Fxd Cer .1 MFD
C304	3954-0004	Cap Fxd Elec 10 MFD
C305	27512-0151	Cap Fxd Mica 150 PFD
C306	76321-0006	Cap Fxd Mylar 2 MFD
C307	3321-9102	Cap Fxd Cer .1 MFD
C308	3954-0004	Cap Fxd Elec 10 MFD
C401	3321-9102	Cap Fxd Cer .1 MFD
C402	27513-0681	Cap Fxd Mica 680 PFD
C403	3321-9102	Cap Fxd Cer .1 MFD
C404	3321-9102	Cap Fxd Cer .1 MFD

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
C405	3321-9102	Cap Fxd Cer .1 MFD
C406	27512-0272	Cap Fxd Mica 2700 PFD
C407	3321-9102	Cap Fxd Cer .1 MFD
C408	3321-9102	Cap Fxd Cer .1 MFD
C409	3321-9102	Cap Fxd Cer .1 MFD
C410	76321-0005	Cap Fxd Mylar .1 MFD
C411	76321-0005	Cap Fxd Mylar .1 MFD
C412	3321-9102	Cap Fxd Cer .1 MFD
C413	27512-0332	Cap Fxd Mica 3300 PFD
C414	23969-0009	Capacitor 1 MFD
C415	3321-9102	Cap Fxd Cer .1 MFD
C416	21485-9101	Cap Fxd Ta 1 MFD
C417	3321-9102	Cap Fxd Cer .1 MFD
C418	24182-0102	Cap Fxd Al 1000 MF 25V
C420	3324-9224	Cap Fxd Mylar .0022 MFD
C443	3321-9102	Cap Fxd Cer .1 MFD
C601	3321-9102	Cap Fxd Cer .1 MFD
C602	3954-0016	Cap Fxd Elec 100 MFD
C603	3321-9102	Cap Fxd Cer .1 MFD
C604	3321-9102	Cap Fxd Cer .1 MFD
C605	3324-9224	Cap Fxd Mylar .0022 MFD
C606	3321-9102	Cap Fxd Cer .1 MFD
C607	3321-9102	Cap Fxd Cer .1 MFD
C608	3324-9103	Cap Fxd Mylar .01 MFD
C609	3324-9224	Cap Fxd Mylar .0022 MFD
C610	3324-9224	Cap Fxd Mylar .0022 MFD
C611	3324-9683	Cap Fxd Mylar .068 MFD
C612	3321-9102	Cap Fxd Cer .1 MFD

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
C613	3321-9102	Cap Fxd Cer .1 MFD
C614	27513-0561	Cap Fxd Mica 560 PFD
C615	27512-0271	Cap Fxd Mica 270 PFD
C616	27512-0271	Cap Fxd Mica 270 PFD
CR401	800-0914	Diode 1N914
CR402	800-0914	Diode 1N914
C403	800-0914	Diode 1N914
CR404	800-0914	Diode 1N914
DS1	76304-0023	Lamp Miniature
E101	610-0093	Terminal, Solder
E102	610-0093	Terminal, Solder
E103	610-0093	Terminal, Solder
E104	610-0093	Terminal, Solder
E106	610-0093	Terminal, Solder
E107	610-0093	Terminal, Solder
E108	610-0093	Terminal. Solder
E201	610-0093	Terminal, Solder
E301	610-0093	Terminal, Solder
E302	610-0093	Terminal, Solder
L401	3422-0222	Inductor 2200 UH
L601	3422-0222	Inductor 2200 UH
L602	3422-0332	Inductor 3300 UH
L603	3422-0681	Inductor 680 UH
L604	3422-0222	Inductor 2200 UH

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
Q101	900-3904	Transistor 2N3904
Q201	900-3904	Transistor 2N3904
Q301	900-3904	Transistor 2N3904
Q302	3431-0023	Transistor TI TIS58
Q303	3431-0023	Transistor TI TIS58
Q304	900-3904	Transistor 2N3904
Q305	900-3904	Transistor 2N3904
Q306	900-3904	Transistor 2N3904
Q401	3431-0025	Transistor MPS 404A
Q402	900-3904	Transistor 2N3904
Q403	900-3904	Transistor 2N3904
Q404	3431-0023	Transistor TI TIS58
Q601	900-3904	Transistor 2N3904
Q602	900-3904	Transistor 2N3904
Q603	3431-0023	Transistor TI TIS58
R101	204-0472	Res Fxd Comp 4.70K
R102	204-0102	Res Fxd Comp 1.00K
R103	204-0102	Res Fxd Comp 1.00K
R104	4567-0013	Res Var Comp 5K
R105	204-0103	Res Fxd Comp 10.0K
R106	204-0103	Res Fxd Comp 10.0K
R107	203-0150	Res Fxd Comp 15 OHM
R108	203-0150	Res Fxd Comp 15 Ohm
R109	204-9561	Res Fxd Comp 5.6 Ohm
R110	204-9821	Res Fxd Comp 8.2 Ohm
R111	204-0102	Res Fxd Comp 1.00K
R112	204-0680	Res Fxd Comp 68 Ohm
R113	204-0473	Res Fxd Comp 47.0K

Reference Designator	Part No.	Description
PCB Assy, Receiver, continued		
R201	204-0100	Res Fxd Comp 10.0 Ohm
R202	204-0102	Res Fxd Comp 1.00K
R203	204-0102	Res Fxd Comp 1.00K
R204	204-0362	Res Fxd Comp 3.6K
R205	204-0362	Res Fxd Comp 3.6K
R206	204-0104	Res Fxd Comp 100K
R207	204-0162	Res Fxd Comp 1.60K
R208	204-0162	Res Fxd Comp 1.60K
R209	204-0100	Res Fxd Comp 10.0 Ohm
R210	204-0270	Res Fxd Comp 27 Ohm
R213	204-9821	Res Fxd Comp 8.2 Ohm
R301	204-0121	Res Fxd Comp 120 Ohm
R302	204-0472	Res Fxd Comp 4.70K
R303	204-0223	Res Fxd Comp 22.0K
R304	204-0472	Res Fxd Comp 4.70K
R305	204-0473	Res Fxd Comp 47.0K
R306	204-0473	Res Fxd Comp 47.0K
R307	204-0391	Res Fxd Comp 390 Ohm
R308	204-0103	Res Fxd Comp 10.0K
R309	204-0472	Res Fxd Comp 4.70K
R310	204-0472	Res Fxd Comp 4.70K
R311	204-0514	Res Fxd Comp 510.0K
R312	204-0394	Res Fxd Comp 390K
R313	204-0106	Res Fxd Comp 10.0 MEG
R314	204-0472	Res Fxd Comp 4.70K
R315	204-0102	Res Fxd Comp 1.00K
R316	204-0102	Res Fxd Comp 1.00K
R317	204-0514	Res Fxd Comp 510K

PCB Assy, Receiver, continued

Reference Designator	TRACOR Part No.	Description
R318	204-0105	Res Fxd Comp 1.00 MEG
R319	204-0106	Res Fxd Comp 10.0 MEG
R320	204-0472	Res Fxd Comp 4.70K
R321	204-0102	Res Fxd Comp 1.00K
R322	204-0102	Res Fxd Comp 1.00K
R323	204-0103	Res Fxd Comp 10.0K
R401	204-0563	Res Fxd Comp 56K
R402	204-0563	Res Fxd Comp 56K
R403	204-0105	Res Fxd Comp 1.00 MEG
R404	204-0205	Res Fxd Comp 2.00 MEG
R405	204-0223	Res Fxd Comp 22K
R406	204-0105	Res Fxd Comp 1.00 MEG
R407	204-0245	Res Fxd Comp 2.4 MEG
R408	204-0473	Res Fxd Comp 47.0K
R409	204-0103	Res Fxd Comp 10.0K
R410	204-0330	Res Fxd Comp 3.30K
R411	204-0102	Res Fxd Comp 1.00K
R412	204-0473	Res Fxd Comp 47.0K
R413	204-0105	Res Fxd Comp 1.00 MEG
R414	204-0205	Res Fxd Comp 2.00 MEG
R415	204-0224	Res Fxd Comp 220.0K
R416	76278-0005	Res Var 50K
R417	204-0224	Res Fxd Comp 220.0K
R418	204-0105	Res Fxd Comp 1.00 MEG
R419	204-0205	Res Fxd Comp 2.00 MEG
R420	204-0334	Res Fxd Comp 330K
R421	204-0105	Res Fxd Comp 1.00 MEG
R422	204-0205	Res Fxd Comp 2.00 MEG

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
R423	212-8060	Res Fxd Film 806 Ohm
R424	212-3163	Res Fxd Film 316K
R425	212-6343	Res Fxd Film 634K
R426	204-0104	Res Fxd Comp 100K
R427	204-0105	Res Fxd Comp 1.00 MEG
R428	204-0205	Res Fxd Comp 2.00 MEG
R429	204-0104	Res Fxd Comp 100K
R430	204-0104	Res Fxd Comp 100K
R431	204-0103	Res Fxd Comp 10K
R432	204-0224	Res Fxd Comp 220K
R433	204-0105	Res Fxd Comp 1.00 MEG
R434	204-0205	Res Fxd Comp 2.00 MEG
R435	204-0102	Res Fxd Comp 1.00K
R436	204-0222	Res Fxd Comp 2.20K
R437	204-0223	Res Fxd Comp 22.0K
R438	204-0223	Res Fxd Comp 22.0K
R439	204-0155	Res Fxd Comp 1.5 MEG
R440	204-0103	Res Fxd Comp 10.0K
R441	204-0820	Res Fxd Comp 82 Ohm
R442	204-0102	Res Fxd Comp 1.00K
R443		Not Used
R444	204-0334	Res Fxd Comp 330K
R445	204-0222	Res Fxd Comp 2.20K
R446	204-0101	Res Fxd Comp 100 Ohm
R447	204-0332	Res Fxd Comp 3.30K
R601	204-0471	Res Fxd Comp 470 Ohm
R602	204-0222	Res Fxd Comp 2.2K
R603	204-0102	Res Fxd Comp 1.00K
R604	204-0682	Res Fxd Comp 6.8K

Reference Designator	TRACOR Part No.	Description
PCB Assy, Receiver, continued		
R605	204-0222	Res Fxd Comp 2.2K
R606	204-0102	Res Fxd Comp 1.0K
R607	204-0220	Res Fxd Comp 22 Ohm
R608	204-0681	Res Fxd Comp 680 Ohm
R609	204-0222	Res Fxd Comp 2.2K
R610	204-0330	Res Fxd Comp 33 Ohm
R611	204-0102	Res Fxd Comp 1.0K
R612	204-0222	Res Fxd Comp 2.2K
R613	204-0332	Res Fxd Comp 3.3K
R614	204-0223	Res Fxd Comp 22.0K
R615	204-0102	Res Fxd Comp 1.00K
R616	204-0332	Res Fxd Comp 3.3K
R617	212-1052	Res Fxd Film 10.5K
R618	212-1052	Res Fxd Film 10.5K
R619	212-5111	Res Fxd Film 5.11K
R620	204-0103	Res Fxd Comp 10.0K
RT401	76457-0001	Thermister
S101	76340-0010	Switch, Toggle
S102	76340-0010	Switch, Toggle
S201	24136-0014	Switch, Toggle
S202	24136-0014	Switch, Toggle
S203	24136-0014	Switch, Toggle
S204	24136-0014	Switch, Toggle
S205	24136-0014	Switch, Toggle
S206	24136-0014	Switch, Toggle
S207	24136-0014	Switch, Toggle
S208	24136-0014	Switch, Toggle
S601	24136-0014	Switch, Toggle

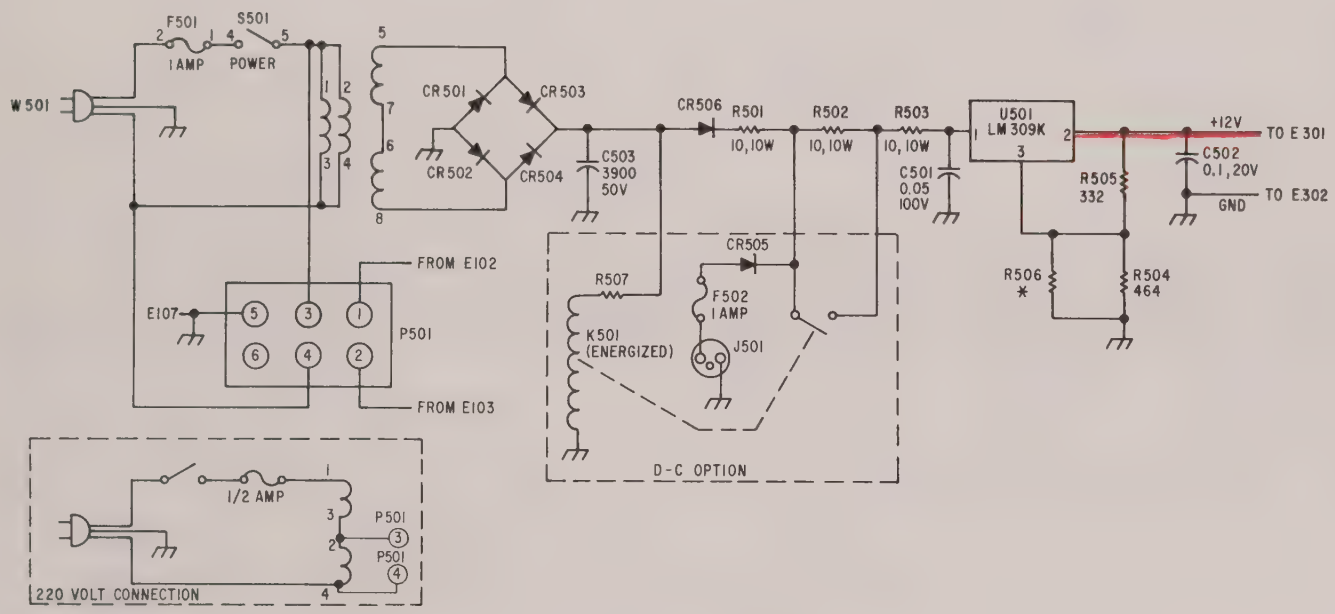
Reference Designator	Part No.	Description
PCB Assy, Receiver, continued		
TP101	610-0093	Terminal, Solder
TP102	610-0093	Terminal, Solder
TP104	610-0093	Terminal, Solder
TP105	610-0093	Terminal, Solder
TP106	610-0093	Terminal, Solder
TP107	610-0093	Terminal, Solder
TP108	610-0093	Terminal, Solder
TP110	610-0093	Terminal, Solder
TP201	610-0093	Terminal, Solder
TP202	610-0093	Terminal, Solder
TP301	610-0093	Terminal, Solder
TP302	610-0093	Terminal, Solder
TP401	610-0093	Terminal, Solder
TP402	610-0093	Terminal, Solder
TP403	610-0093	Terminal, Solder
TP404	610-0093	Terminal, Solder
TP405	610-0093	Terminal, Solder
TP406	610-0093	Terminal, Solder
U101	24201-0090	IC, SN7490N
U102	24201-0090	IC, SN7490N
U103	24201-0090	IC, SN7490N
U104	24201-0090	IC, SN7490N
U105	24201-7400	IC, SN7400N
U106	24201-0002	IC, SN7402N
U107	24201-0073	IC, SN7473N
U108	24201-0090	IC, SN7490N
U109	24201-0090	IC, SN7490N
U110	24201-0121	IC, SN74121N

Reference Designator	Part No.	Description
PCB Assy, Receiver, continued		
U111	24201-0121	IC, SN74121N
U112	24201-0002	IC, SN7402N
U113	24201-7400	IC, SN7400N
U301	76387-0006	Integrated Circuit
U302	76387-0001	IC, LM301AN
U303	76387-0004	Integrated Circuit
U401	76387-0004	Integrated Circuit
U402	76387-0004	Integrated Circuit
U403	76387-0004	Integrated Circuit

Receiver Assy, Model 900 19350-0001

599287-0012	Recorder

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DRN		
	A	REVISED - RELEASED PER DRN 1760	8-1-13	



* 3 SELECTED FOR 12V OUT OF U501
2 ALL CR'S ARE IN4002
1. ALL RESISTORS ARE 1/4 W ± 5% TOL WITH VALUES IN OHMS; CAPACITOR VALUES ARE IN MICROFARADS
NOTES: UNLESS OTHERWISE SPECIFIED

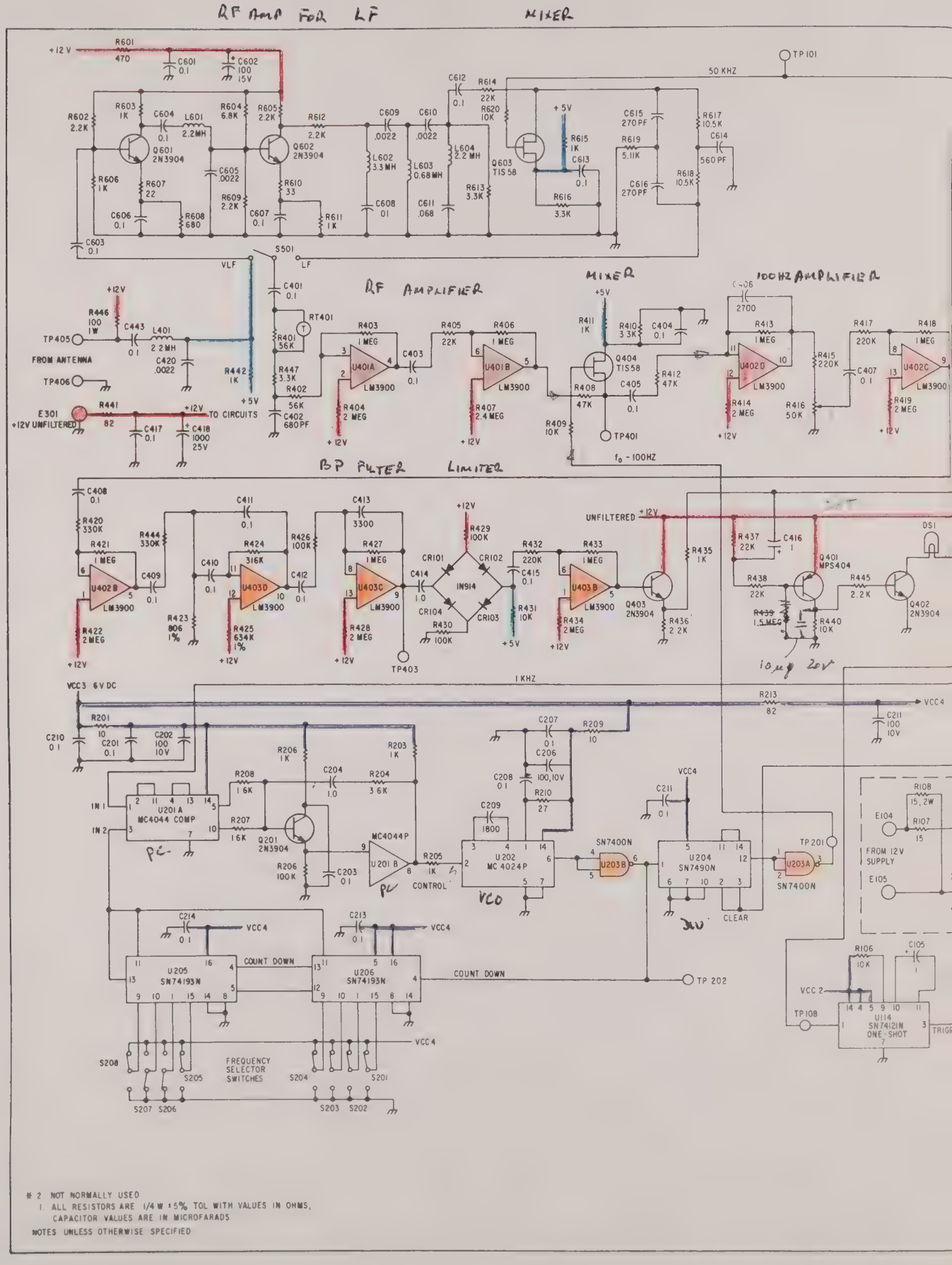
NEXT ASSY	900
APPLICATION	USED ON

ENGINEER		8-1-13
CHECKED		
DRAFTSMAN	MM	3-27-73

TRACOR, INC. AUSTIN, TEXAS

DIAGRAM, SCHEMATIC-CHASSIS

SIZE	CODE IDENT NO.		
B	19397	19356	A
SCALE		SHEET	OF

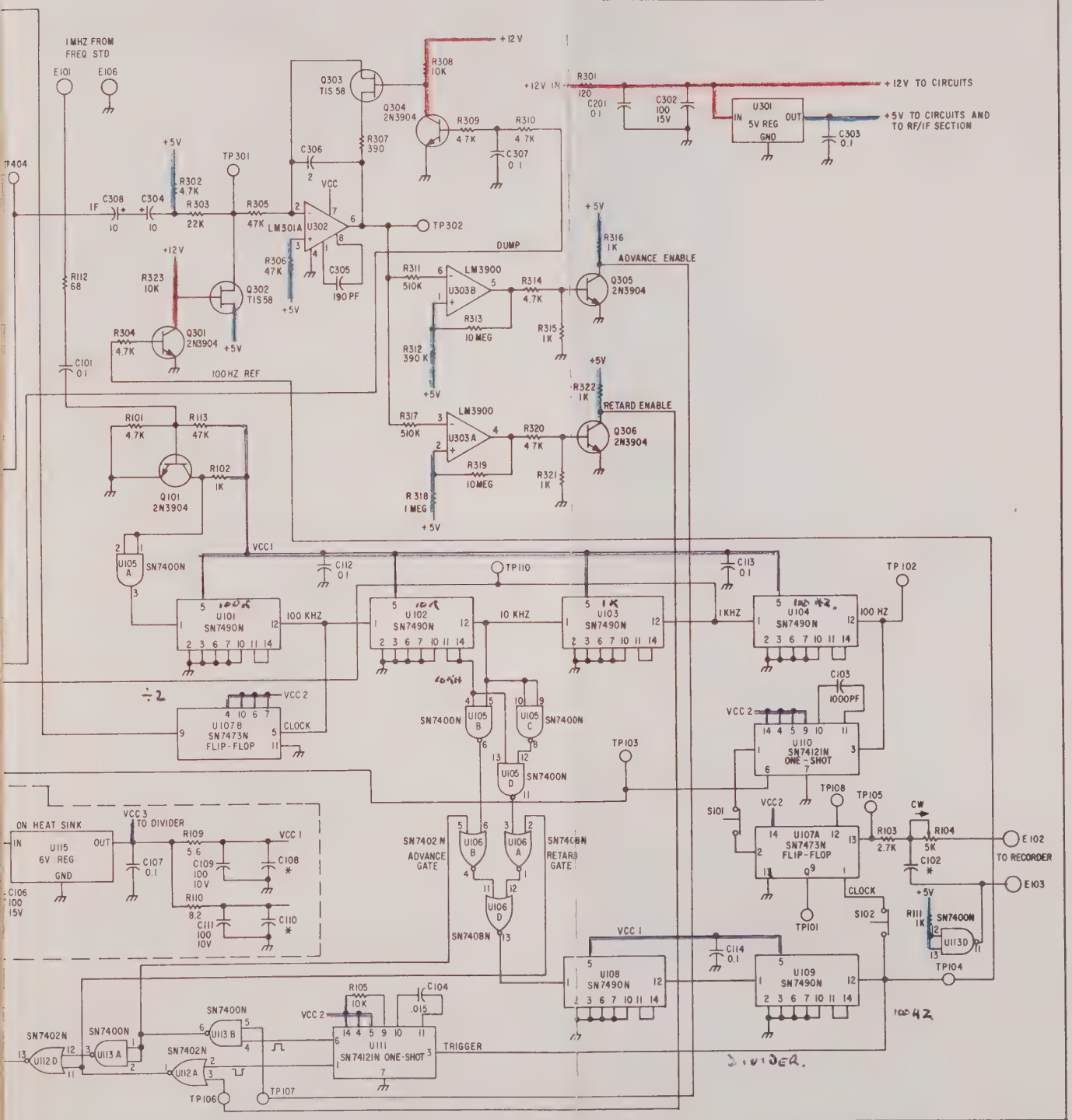


2 NOT NORMALLY USED

1. ALL RESISTORS ARE 1/4 W ±5% TOL WITH VALUES IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS

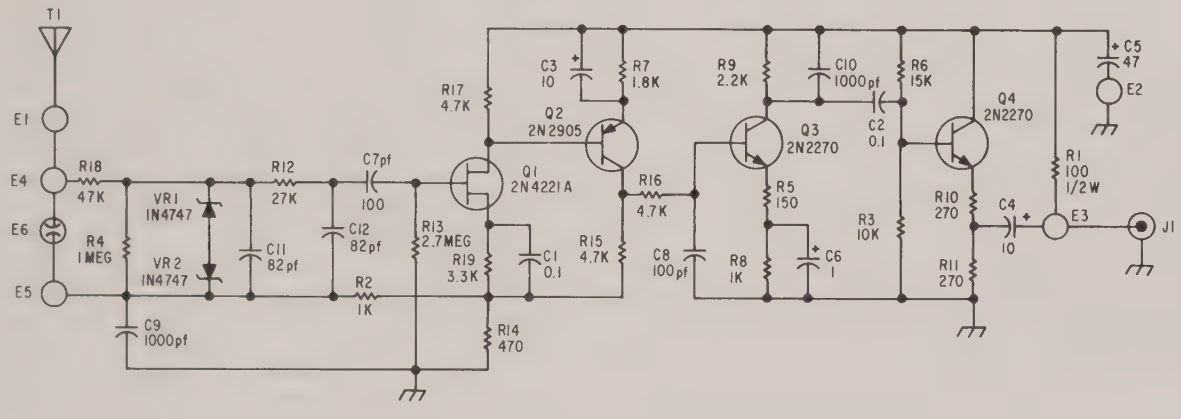
NOTES UNLESS OTHERWISE SPECIFIED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DRN		



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DO NOT SCALE DRAWINGS		TRACOR, INC. AUSTIN, TEXAS
		TOLERANCES UNLESS OTHERWISE SPECIFIED		DIAGRAM, SCHEMATIC RECEIVER, PCB
		DECIMALS / FRACTIONS / ANGLES	ENGINEER	
		MATERIAL:	CHECKED	
			DRAFTSMAN MM 4-2-73	SIZE D / CODE IDENT NO. 19397 / 19357 / -
	900			SCALE / SHEET / OF
NEXT ASSY	USED ON			
APPLICATION				

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	–	RELEASED PER DRN 1760	8-1-73	
	A	CHGD PER ECO 14690	11 2-73	L. KRAUSE



1 ALL RESISTORS ARE 1/4 W ± 5% TOL WITH VALUES IN OHMS, CAPACITOR VALUES ARE IN MICROFARADS

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
	900
APPLICATION	

ENGINEER		8-1-73
CHECKED		
DRAFTSMAN	MM	3-28-73

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DIAGRAM, SCHEMATIC
ANTENNA COUPLER

SIZE	CODE IDENT NO.		
B	19397	19358	A
SCALE		SHEET	OF

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EQUIPMENT NAME _____ MODEL _____

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SUGGESTED ADDITIONS AND DELETIONS

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